REMARKS

Claims 1, 2 and 4-11 are pending in this application. By this Amendment, claims 1, 2 and 4-6 are amended and claims 8-11 are added. Claim 3 is canceled without prejudice to, or disclaimer of, the subject matter recited in that claim. No new matter is added. Reconsideration of this application is respectfully requested.

I. §102 Rejection

The Office Action rejects claims 1, 3 and 7 under 35 U.S.C. §102(b) over Japanese Patent JP 06-027899 to Yamazaki (JP '899). This rejection is respectfully traversed.

Independent claim 1 recites an electro-optical device that includes, among other features, (1) an electrode that is wired to cross a plurality of the data lines and is capacitively coupled with the data lines, (2) an inversion logic circuit with an input terminal supplied with a predetermined level for a bias level, that compares signal levels generated in the electrode to the predetermined level to produce an output value, and (3) logic circuits that selectively adjust a signal supplied to each of a plurality of scanning lines by one of two predetermined amounts based, in part, upon the output value produced by the inversion logic circuit.

Support for the above features may be found throughout the original specification and claims. For example, specific support may be found with respect to exemplary embodiments at least at paragraphs [0063]-[0065], and text related to Fig. 1, Fig. 2, Fig. 5 and Fig. 7. Inversion logic circuit 31 shown in Fig. 1 and Fig. 5 and described at least at paragraph [0087], outputs a logic value of high or low based on whether the electrode voltage DET, e.g., as described in paragraph [0085], is lower than a threshold voltage level or higher than the threshold voltage level, respectively. Further, logic circuit CMP-U 33 and logic circuit CMP-L 34, shown in Fig. 1, each generate high or low values, respectively, as described at paragraphs [0064] and [0065] based, in part, upon the logic output value produced by inversion logic circuit 31. In addition, outputs of logic circuits 33 and 34 result in the

selective addition of predetermined amounts of change to the signal levels supplied to each scanning line, as reflected by the dotted lines in Fig. 7. In the described exemplary embodiment, these predetermined amounts of change are determined by the magnitude of the output of CMP-U (i.e., logic circuit 33), capacitor 36, capacitor 41 and resistor 42, with respect to VSEL' and are determined by the magnitude of the output of CMP-L (i.e., logic circuit 34) capacitor 37, capacitor 43 and resistor 44, with respect to -VSEL', as described at paragraphs [0066]-[0068].

Yamazaki does not teach or suggest such a combination of features. For example, Yamazaki does not teach or suggest an inversion logic circuit, as recited in the claims, capable of producing an output value, as recited in the claims. Further, Yamazaki does not teach or suggest logic circuits that selectively adjust a signal supplied to each of a plurality of scanning lines by one of two predetermined amounts based, in part, upon the output value produced by the inversion logic circuit, as recited in the claims.

For at least these reasons, Yamazaki cannot reasonably be considered to teach or suggest all the features recited in independent claim 1. Claim 7 depends from claim 1 and, therefore, Yamazaki cannot reasonably be considered to teach or suggest all the features recited in claim 7, for at least the reasons addressed above with respect to claim 1 as well as for the additional features that each claim 7 recites. Claim 3 is canceled. Therefore, the rejection is moot with respect to claim 3.

Accordingly, reconsideration and withdrawal of the rejection of claims 1 and 7 under 35 U.S.C. §102(b) over Yamazaki are respectfully requested.

II. §103 Rejection

The Office Action rejects claims 2 and 4-6 under 35 U.S.C. §103(a) as unpatentable over Yamazaki in view of asserted Applicant Admitted Prior Art (AAPA). This rejection is respectfully traversed.

Independent claims 2, 5 and 6 include features similar to those addressed above with respect to claim 1 and, therefore, Yamazaki cannot reasonably be considered to teach or suggest all the features recited in independent claims 2, 5 and 6 for at least the reasons addressed above with respect to claim 1. The AAPA asserted by the Office Action does not overcome the above-described deficiency of Yamazaki with respect to claim 1. Therefore, the asserted combination of Yamazaki and the asserted AAPA cannot reasonably be considered to teach or to suggest the combinations of features recited in claims 2, 5 and 6 for at least the reasons addressed above with respect to claim 1. Claim 4 depends from claim 2 and, therefore, Yamazaki cannot reasonably be considered to teach or suggest all the features recited in claim 4, for at least the reasons addressed above with respect to claim 2 as well as for the additional features that each claim 4 recites.

Accordingly, reconsideration and withdrawal of the rejection of claims 2 and 4-6 under 35 U.S.C. §103(a) over the combination of Yamazaki with AAPA are respectfully requested.

III. New Claims

Claims 8-11 are added. Support for the features of new claims 8-11 may be found throughout the original specification and claims. For example, as addressed above, inversion logic circuit 31 shown in Fig. 1 and Fig. 5 and described at least at paragraph [0087], outputs a logic value of high or low based on whether the electrode voltage DET, e.g., as described in paragraph [0085], is lower than a threshold voltage level or higher than the threshold voltage level, respectively. Further, logic circuit CMP-U 33 and logic circuit CMP-L 34, shown in

Fig. 1, each generate high or low values, respectively, as described at paragraphs [0064] and [0065] based, in part, upon the logic output value produced by inversion logic circuit 31.

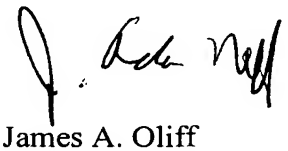
Claims 8-11 depend from independent claims 1, 2, 5 and 6, respectively, and, therefore, no combination of Yamazaki with the asserted AAPA can reasonably be considered to teach or suggest all the features recited in claims 8-11, for at least the reasons addressed above with respect to independent claims 1, 2, 5 and 6, as well as for the additional features that each of claims 8-11 recites.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 2, and 4-11 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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